

FIG. 3

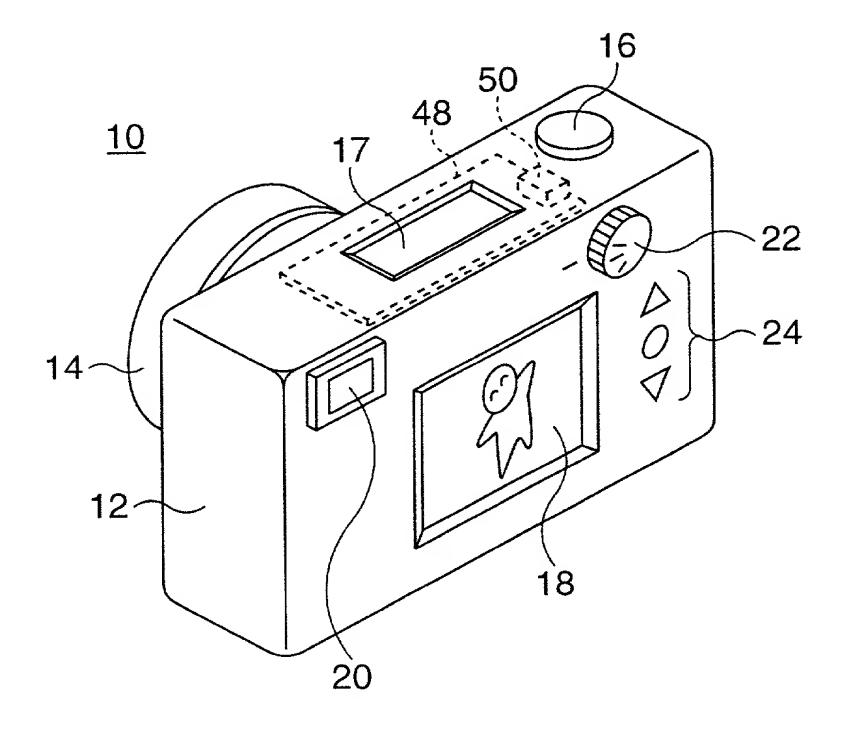
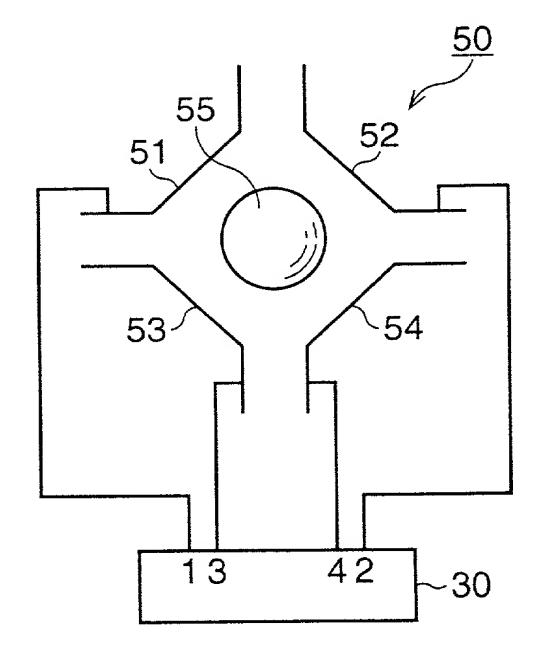


FIG. 4



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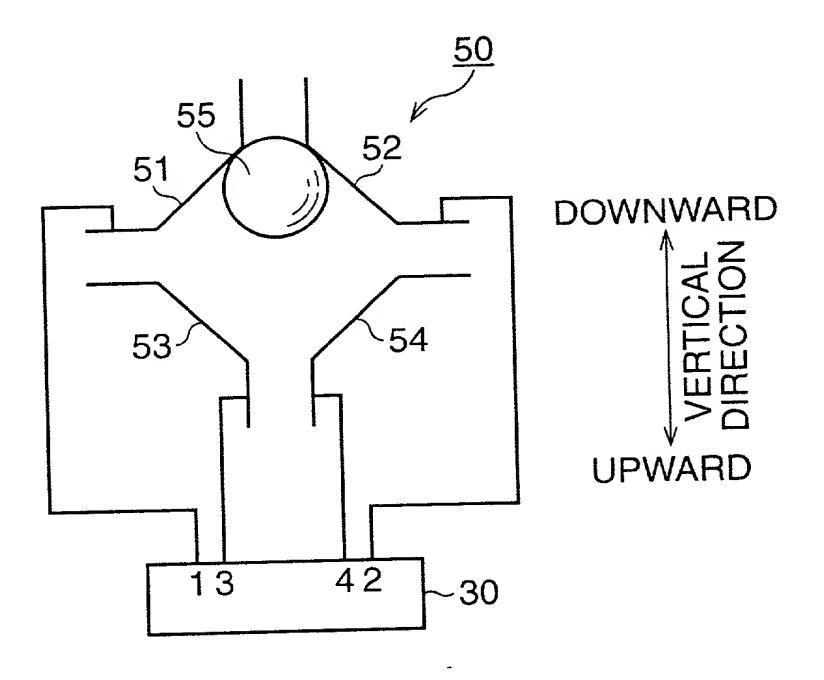
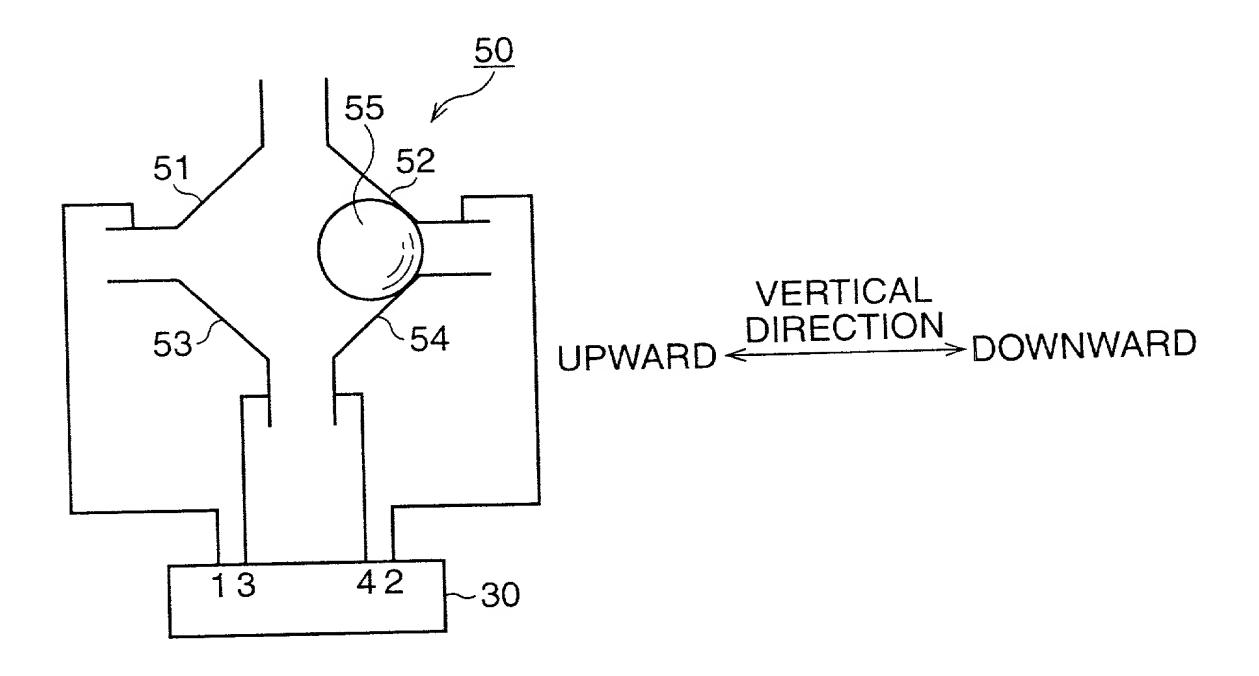


FIG. 6



5/12 FIG. 7

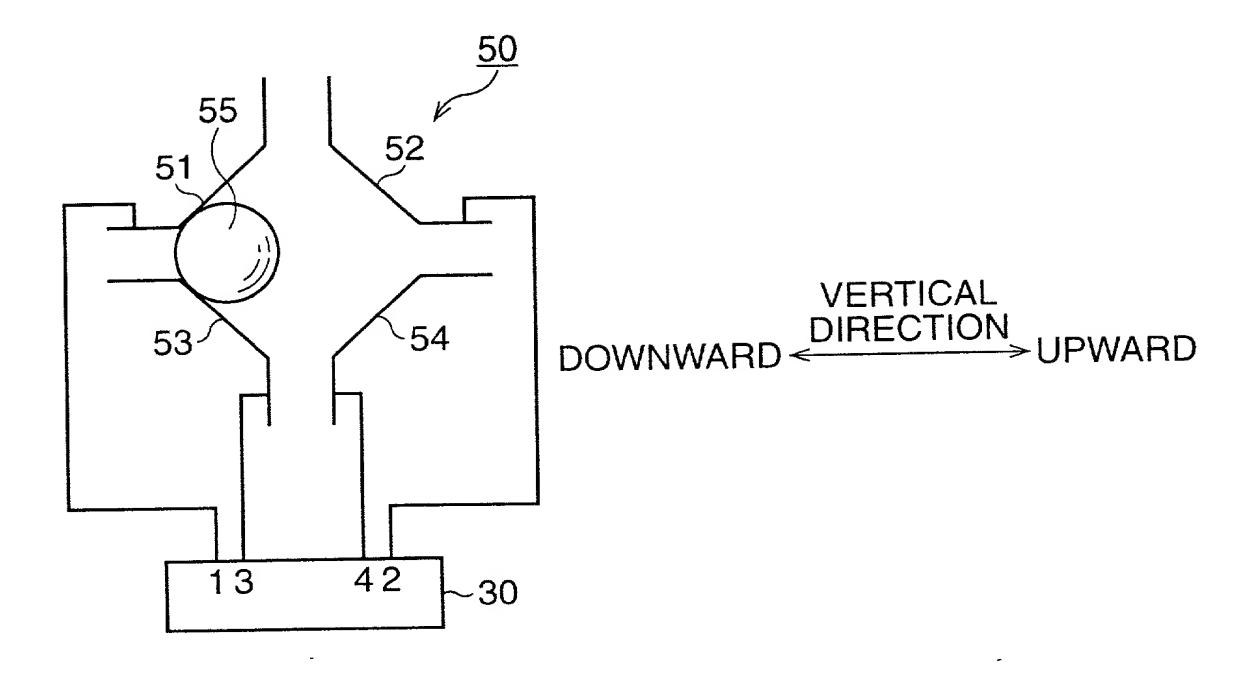
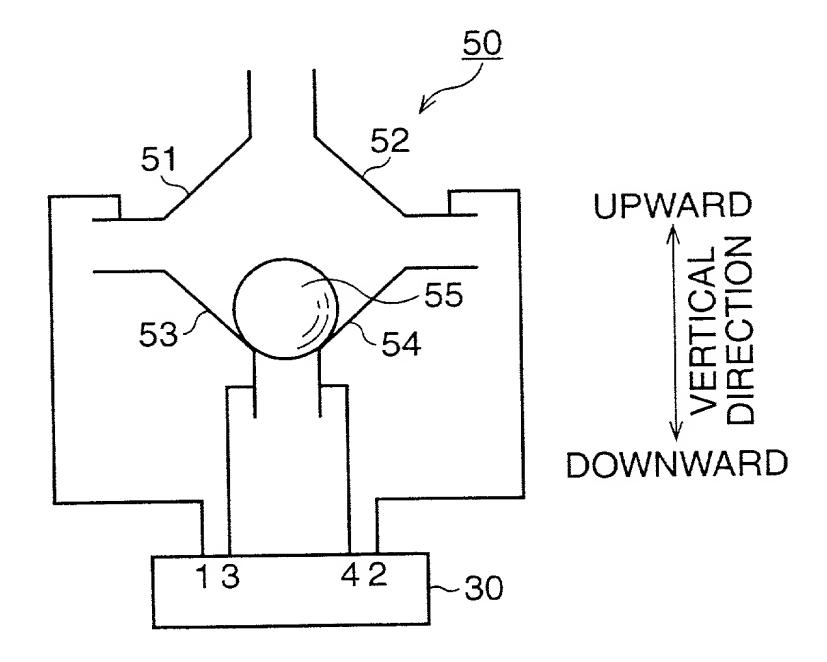
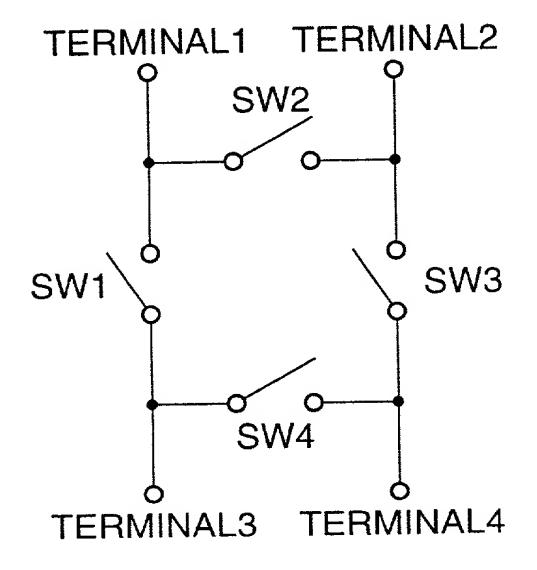


FIG. 8



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SYSTEM CONTROLLER

TERMINAL1

TERMINAL2

SW2

SW3

Q

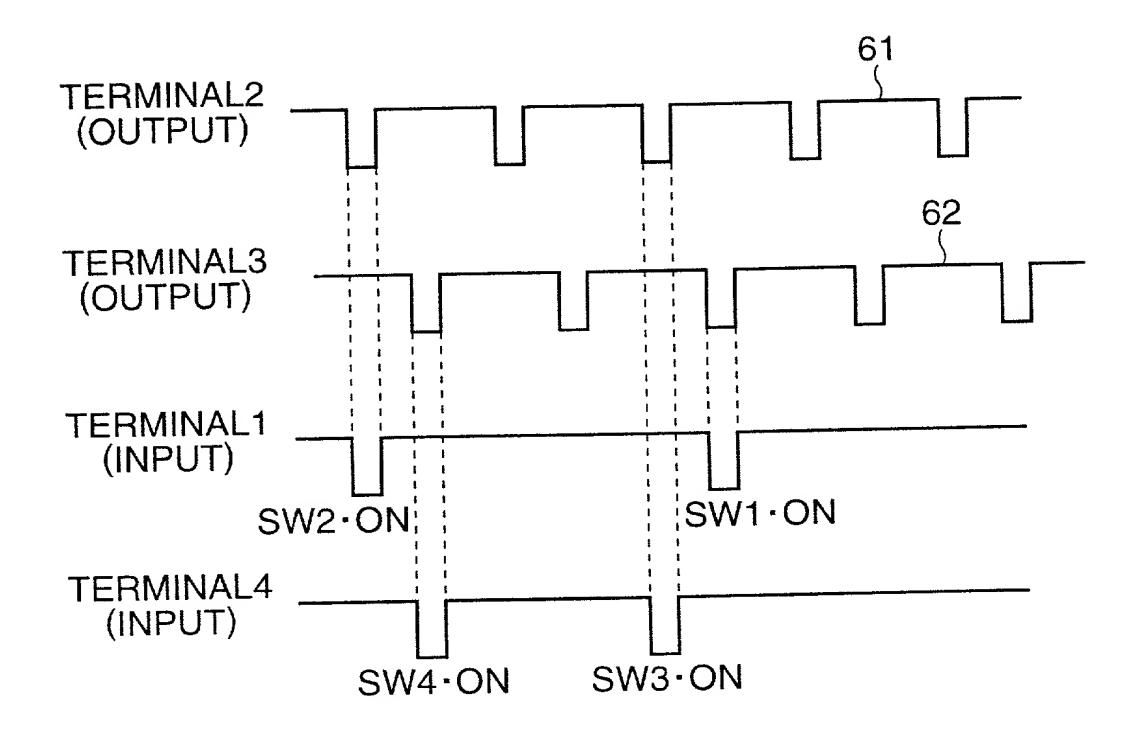
TERMINAL2

SW1

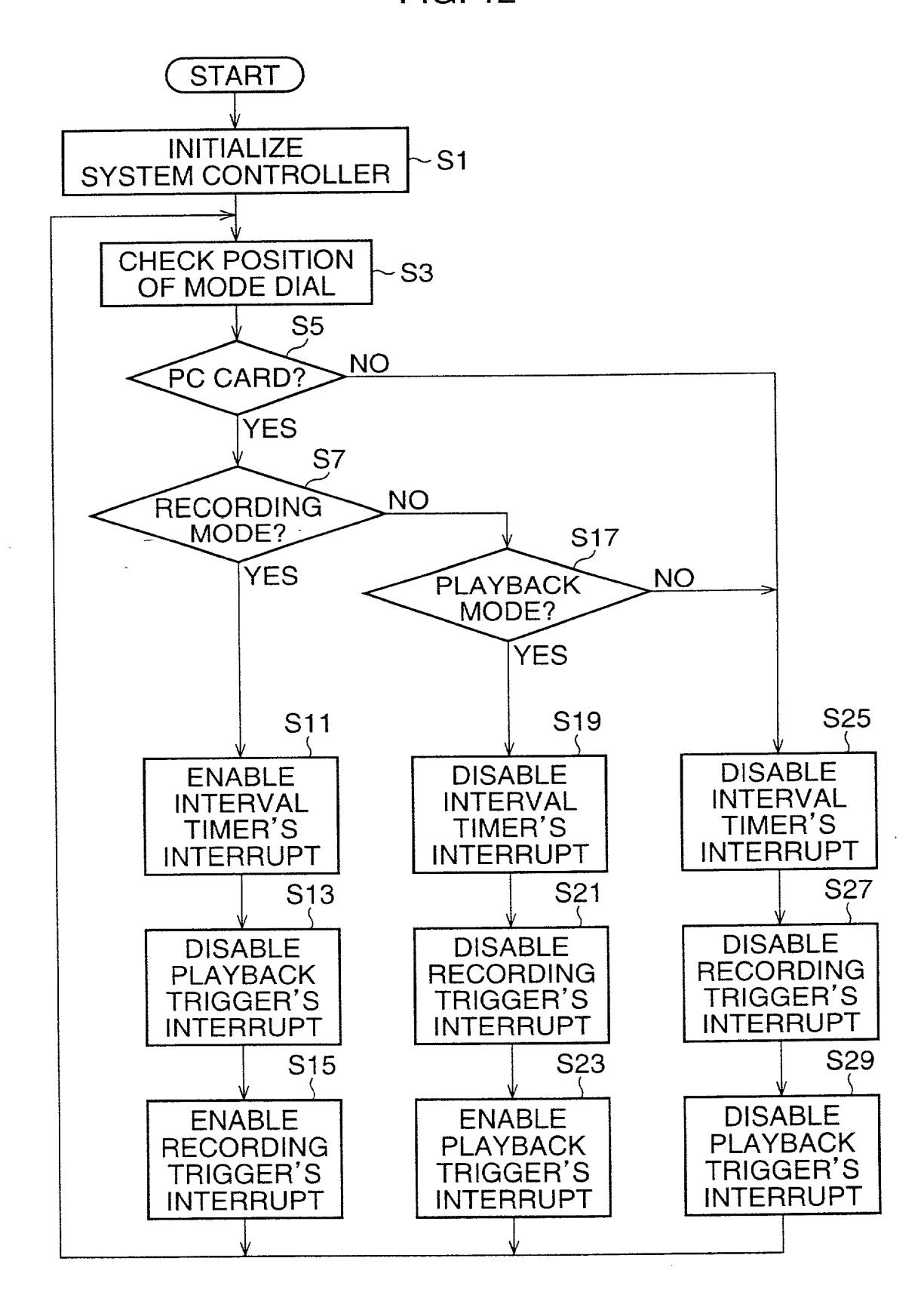
SW4

TERMINAL3

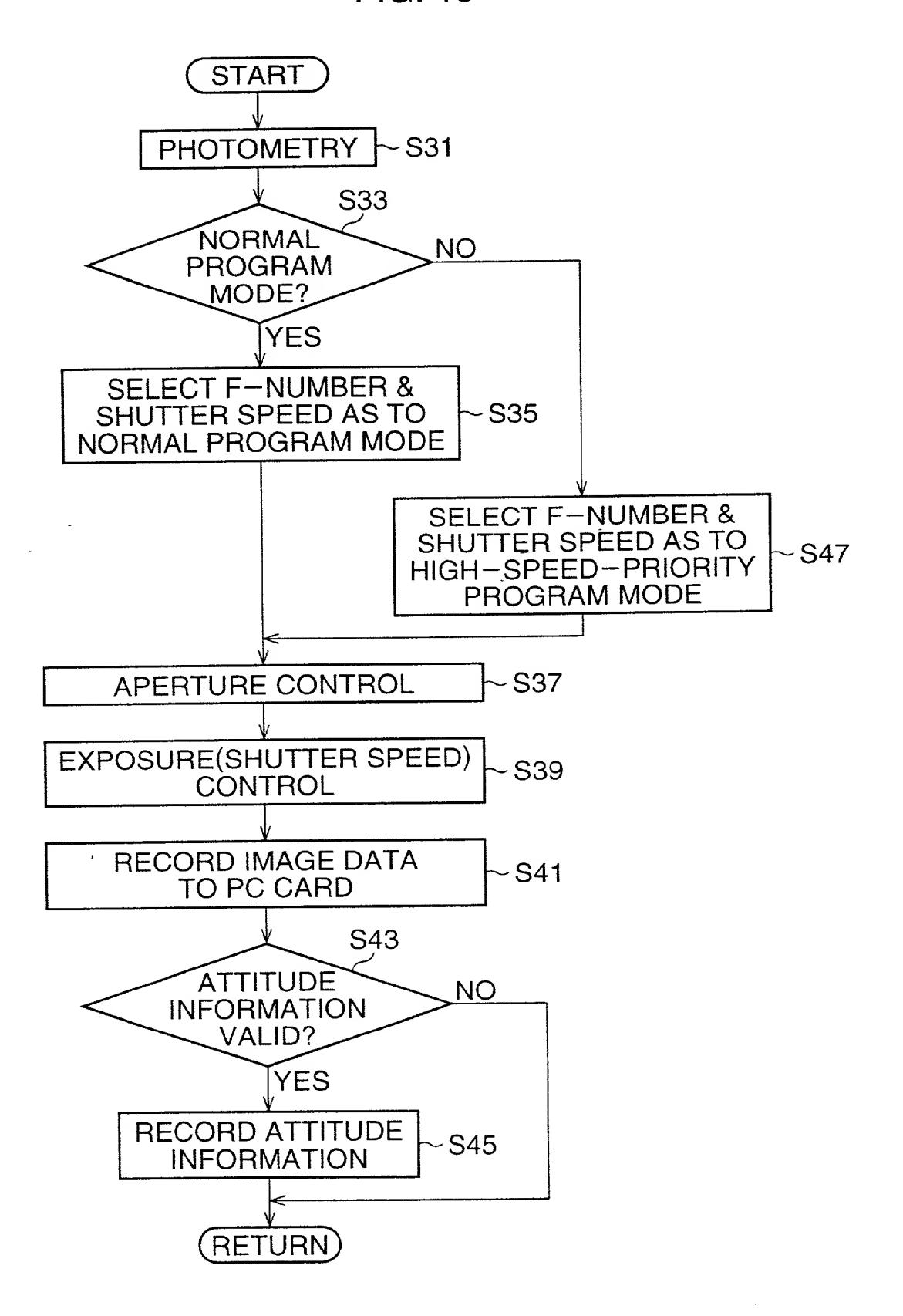
7/12 FIG. 11



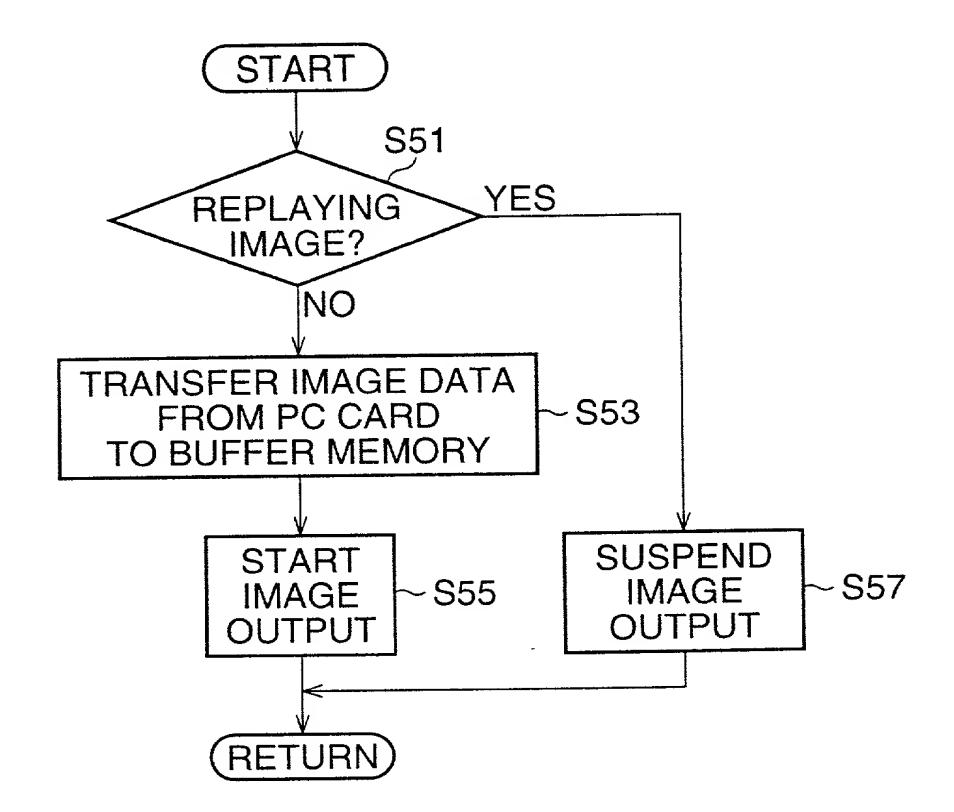
8/12 FIG. 12



9/12 FIG. 13

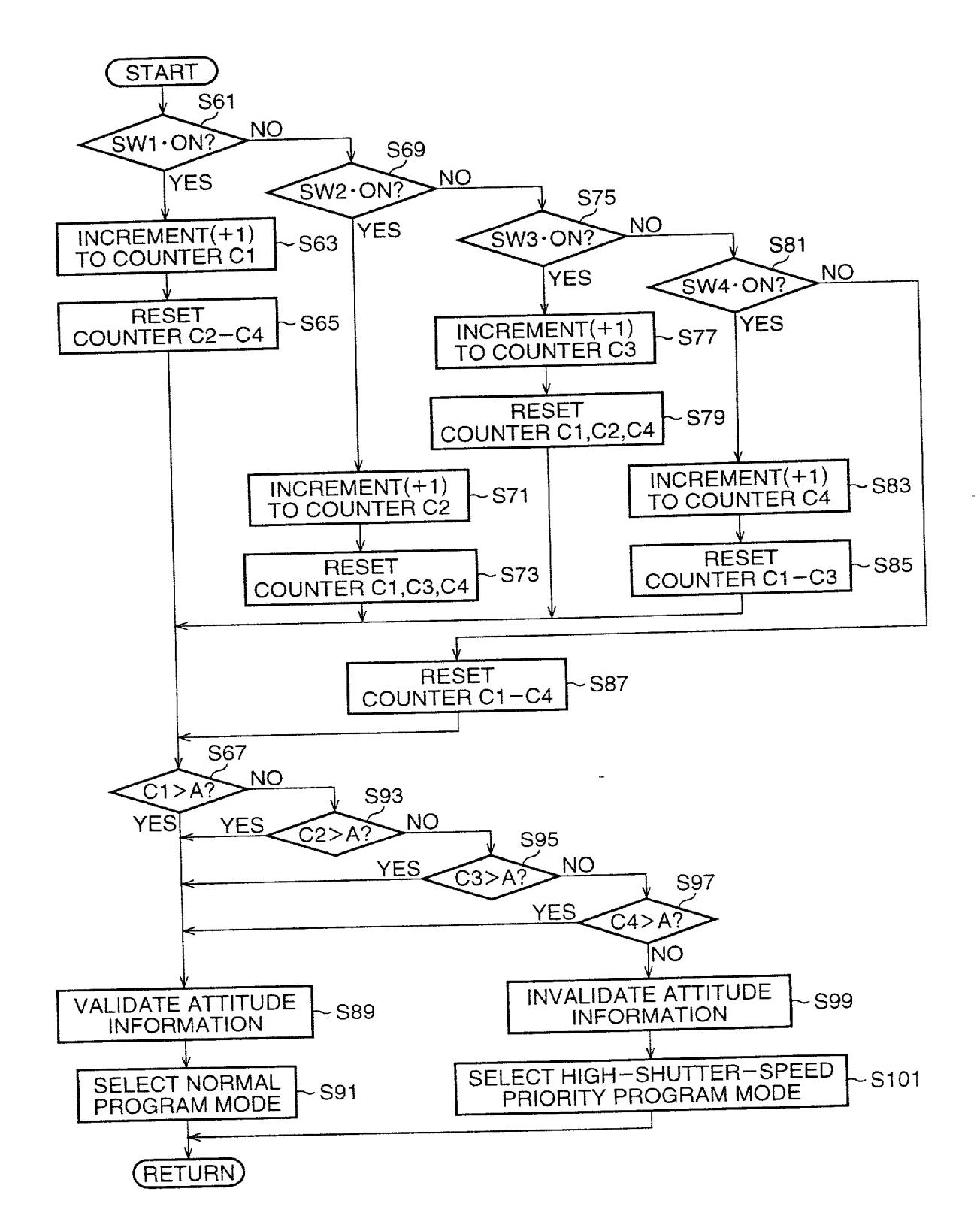


10/12 FIG. 14



7

11/12 FIG. 15



12/12 FIG. 16

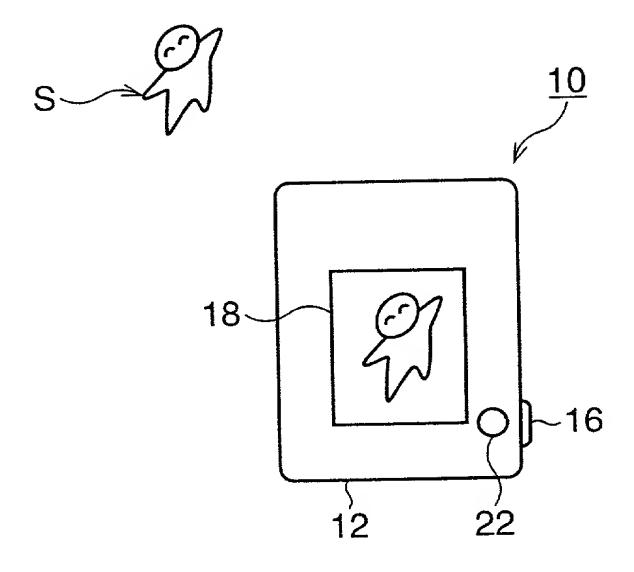


FIG. 17

